CLAIMS

What is claimed is:

1. An analog-to-digital converter (ADC) comprising:

an amplifier comprising an input and an output; and

a switched capacitor network coupled to the input of the amplifier and being coupled to receive an analog input signal and a plurality of reference input signals input to the ADC, the switched capacitor network comprising a plurality of capacitors and switches, each of the plurality of capacitors being coupled to receive at least one of the analog input signal or the reference input signals, wherein the amplifier and switched capacitor network are configured to scale at least one of the plurality of reference input signals by a predetermined scale factor, the predetermined scale factor being determined at least in part by capacitance values of the switched capacitor network, the amplifier and switched capacitor network being further configured to provide an output signal comprising a predetermined gain of the analog input signal adjusted by the predetermined scale factor of the at least one of the plurality of reference input signals.

2. The ADC of claim 1 wherein the plurality of reference input signals includes a first reference input signal and a second reference input signal, the switched capacitor network comprising:

a first capacitor controllably coupled to receive the analog input signal;

a second capacitor controllably coupled to alternately receive the analog input signal or the first reference input signal; and

a third capacitor controllably coupled to receive at least one signal of the analog input signal or the second reference input signal.

3. The ADC of claim 2 wherein capacitance of the first capacitor is designed to be substantially equal to a sum of designed capacitances of the second and third capacitors.

4. The ADC of claim 3 wherein the designed capacitances of the second and third capacitors are substantially equal.

5. The ADC of claim 2 wherein the designed capacitances of the second and third capacitors are substantially equal.

6. The ADC of claim 2 wherein the third capacitor is further controllably coupled to the first reference input signal and a third reference input signal, and wherein:

the third capacitor is coupled to the analog input signal during a first clock phase;

the third capacitor is coupled to the second reference input signal during a second clock phase when the analog input signal is within a first signal range;

the third capacitor is coupled to the first reference input signal during a second clock phase when the analog input signal is within a second signal range; and

the third capacitor is coupled to the third reference input signal during the second clock phase when the analog input signal is within a third signal range.

7. The ADC of claim 6 wherein:

the first capacitor is coupled to the analog input signal during the first clock phase; and

the second capacitor is coupled to the analog input signal during the first clock phase and to the first reference input signal during the second clock phase.

8. The ADC of claim 6 wherein the first signal range includes voltage potentials higher than voltage potentials of the second signal range and the third signal range, and the third signal range includes voltage potentials lower than voltage potentials of the first signal range and the second signal range, the predetermined gain being negative when the analog input signal is in the first signal range, the predetermined gain being positive when the analog input signal is in the third signal range.

9. The ADC of claim 8 wherein the third reference input signal has a higher potential than potentials of the first and second reference input signals.

10. The ADC of claim 2 wherein the first capacitor is controllably coupled to receive a feedback signal from the output of the amplifier.

11. The ADC of claim 2 wherein at least one of the first reference input signal or the second reference input signal is a power supply signal.

12. The ADC of claim 2 wherein the first reference input signal and the second reference input signal are both ground signals.

13. The ADC of claim 2 wherein the third capacitor is further controllably coupled to the first reference input signal but not connected to the analog input signal, and wherein:

the first capacitor is coupled to the analog input signal during a first clock phase;

the second capacitor is coupled to the analog input signal during the first clock phase; and

the second capacitor is coupled to the first reference input signal during a second clock phase.

14. The ADC of claim 13 wherein:

the third capacitor is coupled to the first reference input signal during a first selected one of the first clock phase or the second clock phase; and

the third capacitor is coupled to the second reference input signal during a second selected one of the first clock phase or the second clock phase.

15. The ADC of claim 13 wherein:

the first capacitor is coupled to a feedback signal from the output of the amplifier during a second clock phase.

16. The ADC of claim 13 further comprising:

first and second switches, wherein the third capacitor is controllably coupled to the first reference input signal or the second reference input signal depending on conductive states of respective first and second switches; and

a control circuit for selecting a first set of states of the first and second switches during a first clock phase and for alternately selecting a second set of states of the first and second switches during the first clock phase.

17. The ADC of claim 1 comprised within an integrated circuit, wherein the predetermined scale factor is selectable after power is provided to the integrated circuit, the predetermined scale factor being selectable from a range of scale factors including a scale factor of one.

18. The ADC of claim 1 further comprising at least one RSD stage, each of the at least one RSD stage comprising a respective amplifier and a switched capacitor network.

19. The ADC of claim 1 further comprising a plurality of ADC stages coupled in series, each of the plurality of ADC stages including a respective amplifier and a switched capacitor network.

20. The ADC of claim 19 wherein the ADC is a cyclic analog-to-digital converter (ADC) and wherein each ADC stage is a redundant signed digit (RSD) stage.

21. The ADC of claim 19 further comprising a plurality of multiplying digital to analog converters (MDACs), each of the plurality of ADC stages including a respective one of the plurality of MDACs, each of the plurality of MDACs including a respective amplifier and switched capacitor network.

22. The ADC of claim 1 further comprising a multiplying digital to analog converter (MDAC), the MDAC including the amplifier and the switched capacitor network.

23. In an analog-to-digital converter (ADC), a processing and scaling circuit comprising:
an amplifier comprising an input and an output, the amplifier having operational range within a power supply range; and
a switched capacitor circuit coupled to the input of the amplifier and the output of the amplifier, the switched capacitor circuit comprising:
an analog signal input node for receiving an analog signal;
a reference input node for receiving a reference signal capable of having a value outside the operational range of the amplifier;
a plurality of capacitance elements, each of the plurality of capacitance elements being controllably coupled to at least one of the analog signal input node or the reference input node and being controllably coupled to the input of the amplifier; wherein,
the amplifier and switched capacitor circuit, responsive to receiving the analog signal and the reference signal, scale the reference signal by a predetermined scale factor to provide a scaled reference signal within the operational range of the amplifier, and process the analog signal to provide an output signal having a predetermined gain of the analog signal adjusted by the predetermined scale factor of the reference signal.

24. The ADC of claim 23 wherein the switched capacitor circuit further comprises:
first, second and third capacitors, each having first and second terminals;
a first switch coupled between the first terminal of the first capacitor and the analog signal input node;
a second switch coupled between the first terminal of the second capacitor and the analog signal input node;
a third switch coupled between the first terminal of the second capacitor and a first power supply signal terminal; and
a fourth switch coupled between the first terminal of the third capacitor and the reference input node.

25. The ADC of claim 24 wherein the first and second capacitors are coupled to receive the analog signal and the third capacitor is not coupled to receive the analog signal.

26. The ADC of claim 24 further comprising:

a fifth switch coupled between the input of the amplifier and at least one of the second terminals of the first, second and third capacitors; and

a sixth switch coupled between the first power supply signal terminal and at least one of the second terminals of the first, second and third capacitors.

27. The ADC of claim 26 wherein

the first, second and sixth switches are controlled to close the first, second and sixth switches during a first clock phase; and

the third and fifth switches are controlled to close the third and fifth switches during a second clock phase.

28. The ADC of claim 27 further comprising:

a seventh switch coupled between the first terminal of the third capacitor and the first power supply signal terminal; wherein,

the seventh switch is controlled to close the seventh switch during a first selected one of the first clock phase and the second clock phase; and

the fourth switch is controlled to close the fourth switch during a second selected one of the first clock phase and the second clock phase.

29. The ADC of claim 24 wherein the switched capacitor circuit further comprises:

first, second and third capacitors, each having first and second terminals;

a first switch coupled between the first terminal of the first capacitor and the analog signal;

a second switch coupled between the first terminal of the second capacitor and the analog signal input node;

a third switch coupled between the first terminal of the third capacitor and the analog signal input node;

a fourth switch coupled between the first terminal of the second capacitor and the first power supply signal terminal; and

a fifth switch coupled between the first terminal of the third capacitor and the reference input node.

30. The ADC of claim 29 wherein

a sixth switch coupled between the input of the amplifier and at least one of the second terminals of the first, second and third capacitors; and

a seventh switch coupled between the first power supply signal terminal and the at least one of the second terminals of the first, second and third capacitors.

31. The ADC of claim 29 wherein

the sixth and fourth switches are controlled to close the sixth and fourth switches during a first clock phase; and

the first, second, third and seventh switches are controlled to close the first, second, third and seventh switches during a second clock phase.

32. The ADC of claim 31 wherein the reference signal is a first reference signal, the ADC further comprising:

an eighth switch coupled between the first terminal of the third capacitor and a second reference signal terminal; wherein,

the fifth switch is controlled to close the fifth switch during the first clock phase when the analog signal is in a first range; and

the eighth switch is controlled to close the eighth switch during the first clock phase when the analog signal is in a second range.

33. The ADC of claim 32 wherein

a second reference signal coupled to the second reference signal terminal has a lower potential than the first reference signal; and

the first range includes higher voltage potentials than the second range.

34. The ADC of claim 33 further comprising:

a ninth switch coupled between the first terminal of the third capacitor and the first power supply signal terminal, wherein the ninth switch is controlled to close during the first clock phase when the analog signal is in a third range, the third range including potentials lower than the first range and higher than the second range.

35. The ADC of claim 34 wherein the second reference signal and the power supply signal are coupled to ground potential.

36. The ADC of claim 24 wherein the switched capacitor circuit further comprises a feedback input node coupled to receive an amplifier feedback signal, and the first terminal of the first capacitor is controllably coupled to alternately receive the analog signal and the amplifier feedback signal.

37. The ADC of claim 24 wherein the predetermined scale factor is selected from a range of scale values including a scale value of one.

38. The ADC of claim 24 wherein the reference signal is one of a plurality of reference signals, the plurality of reference signals comprising a maximum power potential and a minimum power potential.

39. The ADC of claim 38 wherein the minimum power potential is ground potential.

40. The ADC of claim 24 wherein the reference signal is one of at least three reference signals, the at least three reference signals comprising a maximum reference signal, a minimum reference signal, and middle reference signal, the middle reference signal being at a potential between potentials of the maximum and minimum reference signals.

41. The ADC of claim 24 wherein the reference signal is one of a plurality of reference signals, the plurality of reference signals comprising first and second voltage signals configured for derivation from a bandgap voltage.

42. The ADC of claim 23 comprising:

first and second power supply inputs, wherein the amplifier is coupled to receive first and second power supply signals, and the reference signal is one of the first and second power supply signals.

43. In a system for analog-to-digital conversion, a method for processing an analog signal, the method comprising:

receiving an analog signal at an analog-to-digital conversion (ADC) stage;

receiving an unscaled reference signal at the ADC stage;

generating a scaled reference signal from the unscaled reference signal by a switched capacitance and amplification circuit of the ADC stage; and

generating and outputting a processed signal from the analog signal and the scaled reference signal by alternately coupling the analog signal and the unscaled reference signal to capacitors of the switched capacitance and amplification circuit.

44. A method of scaling a signal for use by a data converter, the method comprising:

receiving an input signal having a first operating range of voltages;

receiving a reference potential;

providing the input signal and the reference potential to a switched capacitor network comprising switched capacitors and an amplifier;

scaling the reference potential by a predetermined scale factor determined by capacitive values within the switched capacitor network to provide a scaled reference signal within a second operating range of voltages; and

processing the input signal also with the switched capacitor network to provide an output signal comprising a predetermined gain of the input signal adjusted by the scaled reference signal.

45. The method of claim 44 wherein the first operating range of voltages corresponds to a range between two power supply potentials and voltages of the second operating range are substantially within the first operating range.

46. The method of claim 44 wherein the data converter comprises an analog-to-digital converter (ADC) and the input signal is an analog signal, the method further comprising:

converting the analog signal to a digital signal using the scaled reference signal.

47. The method of claim 44 further comprising:

allowing a user of the data converter to programmably control the predetermined scale factor.